# A Broadband and High-Efficiency Microbump Antenna-on-Chip Based on Parasitic-Mode Control With Ultra-Thin Substrate

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***Abstract*—Microbump antenna offers a viable antenna-on-chip (AoC) solution to achieve high radiation efficiency using standard semiconductor processes. This letter presents a feasible method for broadening the bandwidth of terahertz microbump antenna while preserving its high efficiency. Instead of introducing additional microbump structures, two pairs of lossy parasitic strips are used to introduce high-efficiency parasitic resonance, while enabling differential mode in each strip pair to mitigate the in-band gain deterioration. The proposed antenna is fabricated using the 65 nm complementary metal-oxide-semiconductor process and the standard flip-chip technology. Compared with the existing on-chip microbump antennas, the proposed method enhances the bandwidth from 2.8% to 5.7% , achieving an efficiency of 42% and a gain of 3.85 dBi on a substrate with a thickness of $0.006\lambda_0$, providing an implementable solution for high-performance AoCs for subterahertz integrated circuits.**

***Index Terms*—Antenna-on-chip (AoC), broadband antennas, flip chip, microbump antennas, terahertz antenna.**

## I. Introduction

THE terahertz (THz) band (0.3–10 THz) offers unique potential for ultra-high-speed wireless links, submillimeter imaging, and noncontact security screening [1], [2], [3]. Standard complementary metal-oxide-semiconductor (CMOS) technology, with its low cost, high integration density, and design compatibility, enables monolithic THz system-on-chip solutions integrating transceivers, processors, and antennas [4]. In such systems, Antenna-on-Chip (AoC) designs are vital for compact, low-loss integration with active circuits [5]. However, at THz frequencies, metal losses and the ultra-low profiles imposed by CMOS metal layer constraints severely limit AoC efficiency and bandwidth [6], [7].

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Previous works have focused on improving the bandwidth of AoCs [8], [9], [10]. Recently, a 425 GHz on-chip circularly polarized antenna with 19% axial-ratio bandwidth is proposed in [9]. In [10], a broadband circularly polarized loop antenna is realized using a parasitic ring. However, constrained by CMOS processes, the antennas proposed in these studies typically feature low-profile structures, which in turn lead to limited radiation efficiency.

To enhance the efficiency and bandwidth of AoCs, various postprocessing techniques have been explored to overcome the limitations of standard semiconductor fabrication processes [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. Among them, adding a superstrate or resonator above the antenna has proven effective, such as quartz superstrates with high dielectric constant [11], [12], stacked dielectric resonators [13], and electrically large package-level lenses [14], [15], all of which can significantly improve gain and radiation efficiency. In addition, substrate modification techniques, including localized backside etching and through-silicon vias, have been employed to reduce substrate loss [16], [17]. Artificial dielectric layers have also been reported to improve the front-to-back ratio of printed antennas [18], [19], while bond-wire-based monopole antennas offer another route to achieving high radiation efficiency [20]. While dielectric resonator antennas and superstrate-based designs can improve the radiation performance of AoCs, they often require manual assembly or specialized packaging modifications, which increase fabrication complexity and cost, and may limit yield and scalability in commercial semiconductor workflows [22].

Recently, the authors in [23] and [24] proposed the concept of the microbump antenna and established its theoretical operation in transverse magnetic (TM) modes by placing a solder bump on a patch via a standard flip-chip process. A 283-GHz microbump antenna was designed and fabricated in [22], demonstrating that the hybrid electromagnetic $HEM_{11}$ mode can enhance radiation efficiency from 15.9% to 41.1% compared with the $TM_{01}$ patch mode, highlighting microbump antennas as a promising solution for high-efficiency AoCs. Furthermore, due to its reliance on a flip-chip process that is fully compatible with standard CMOS technology, the microbump antenna supports low-cost manufacturing [25]. However, for a microbump antenna, the solder ball occupies the majority of the original patch area, making other methods to broaden bandwidth—such as introducing slots on the patch to achieve higher order mode coupling—inapplicable. This necessitates a solution that can extend the

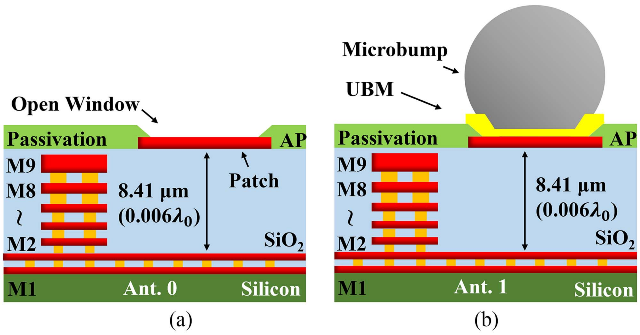


Fig. 1. Cross view of (a) a typical microstrip antenna with an open window in 65 nm CMOS process and (b) a microbump antenna with flip-chip assembly.

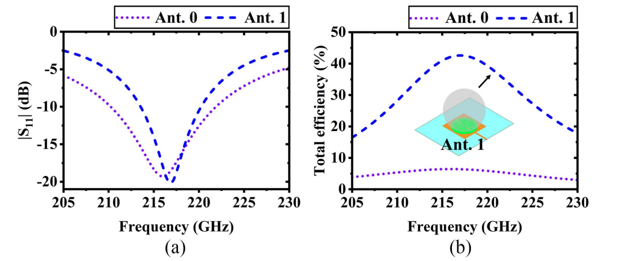


Fig. 2. (a) Simulated reflection coefficients of Ant. 0 and Ant. 1. (b) Simulated total efficiency of Ant. 0 and Ant. 1.

bandwidth of the microbump antenna while preserving its hard-won high radiation efficiency.

In this letter, a feasible bandwidth-enhancement method based on parasitic-mode excitation is proposed for terahertz microbump antennas, while preserving their hard-won high radiation efficiency and without introducing additional microbump structures. Through a systematic evolution of the parasitic strip configuration, a pair of dual L-shaped parasitic strips is ultimately employed to introduce an additional high-efficiency parasitic resonant mode. Compared with conventional microbump antenna designs, the proposed solution significantly expands the impedance bandwidth from 2.7% to 5.7% on an ultra-thin substrate with a thickness of only $0.006\lambda_0$ (where $\lambda_0$ is the free-space wavelength at the center frequency). Moreover, the antenna achieves a measured peak gain of 3.85 dBi and a simulated peak total radiation efficiency of 42% , demonstrating an effective bandwidth–efficiency enhancement strategy that can be directly applied to existing microbump antenna designs.

## II. Structure of Typical Microbump Antenna

Fig. 1(a) and (b) illustrates the stack-up of a rectangular microstrip antenna (Ant. 0) and a typical microbump antenna (Ant. 1) implemented in a 65-nm CMOS process. The antenna is fabricated on the aluminum pad (AP) metal layer, which also serves as the I/O pad, while the ground plane is realized on M2. The vertical spacing between the AP and M2 layers is 8.41 $\mu$m. The silicon substrate exhibits a dielectric constant of 11.9 and a resistivity of 10–15 Ω·cm. A 200-$\mu$m-diameter opening in the passivation layer exposes the I/O pad for interconnection. As shown in Fig. 1(b), an Sn–Ag chip connection (C4) solder ball is used as the microbump antenna element. The microbump is connected to the I/O pad through an underbump metallization layer.

In both Ant. 0 and Ant. 1, the patch dimensions are identical, with a length of 328 $\mu$m and a width of 310 $\mu$m. When the microbump is introduced, the $\mathrm{HEM}_{11}$ mode is also excited [22]. According to the sphere models, the resonant frequency of the $\mathrm{HEM}_{11}$ mode can be approximated as [23]

$$f_{11} = \frac{552.36}{2\pi l_p \cdot \sqrt{\varepsilon_e}} \tag{1}$$

where $\varepsilon_e$ and $l_p$ denotes the effective dielectric constant and the length of patch, respectively. The microbump in Ant. 1 has a radius of 200 $\mu$m and a height of 340 $\mu$m. The simulated $S_{11}$ and total efficiency of Ant. 0 and Ant. 1 are shown in Fig. 2(a) and (b). As shown in Fig. 2(b), conventional microstrip antennas on the 0.006 $\lambda_0$-thick substrate exhibit efficiencies below 10% , mainly due to the high-Q and lossy cavity resonance at THz frequencies [9]. By contrast, introducing the microbump increases the total efficiency to 43% , owing to its much higher effective profile, which reduces surface current density and ohmic loss.

## III. Evolution Process

### A. Bandwidth Enhancement

The evolution of the proposed antenna from Ant. 1 to Ant. 4 is illustrated in Fig.3(a) . Since the microbump occupies a substantial portion of the patch area, introducing additional resonant structures is considered as a strategy to broaden the bandwidth of microbump antenna. As shown in Fig. 3(b), a pair of straight parasitic strips is introduced symmetrically on both sides of the microbump. As observed in Fig. 3(e), an additional parasitic resonance is excited in the vicinity of the intrinsic $\mathrm{HEM}_{11}$ mode, which extends the impedance bandwidth from 214–220 GHz (2.7% ) to 212.5–225 GHz (5.7% ).

However, as shown in Fig. 3(f) and (g), a sharp drop in the simulated total efficiency is observed at 224 GHz, where the in-band efficiency decreases by approximately 17% , accompanied by a gain reduction of more than 2.6 dB. This degradation in efficiency is attributed to the differential mode resonance between the parasitic strips and the microbump at this frequency, as depicted in Fig. 3(b). Specifically, the parasitic strips are excited via magnetic coupling, which induces a current distribution that is out of phase with the current on the microbump. This phase opposition results in partial radiation cancellation, thereby causing a dip in radiation efficiency.

### B. Efficiency Improvement

To address the efficiency degradation issue, the straight parasitic strips are replaced with L-shaped strips. As shown in Fig. 3(c), the location of the strongest resonant current on the parasitic strips is shifted to the corner of the L-shape, moving it away from the region of maximum current on the microbump. As shown in Fig. 3(f) and (g), the in-band efficiency and gain degradation are alleviated. However, at 220 GHz, an efficiency reduction of approximately 12% and a gain drop exceeding 1.5 dB are still observed, which remain undesirable for practical system applications.

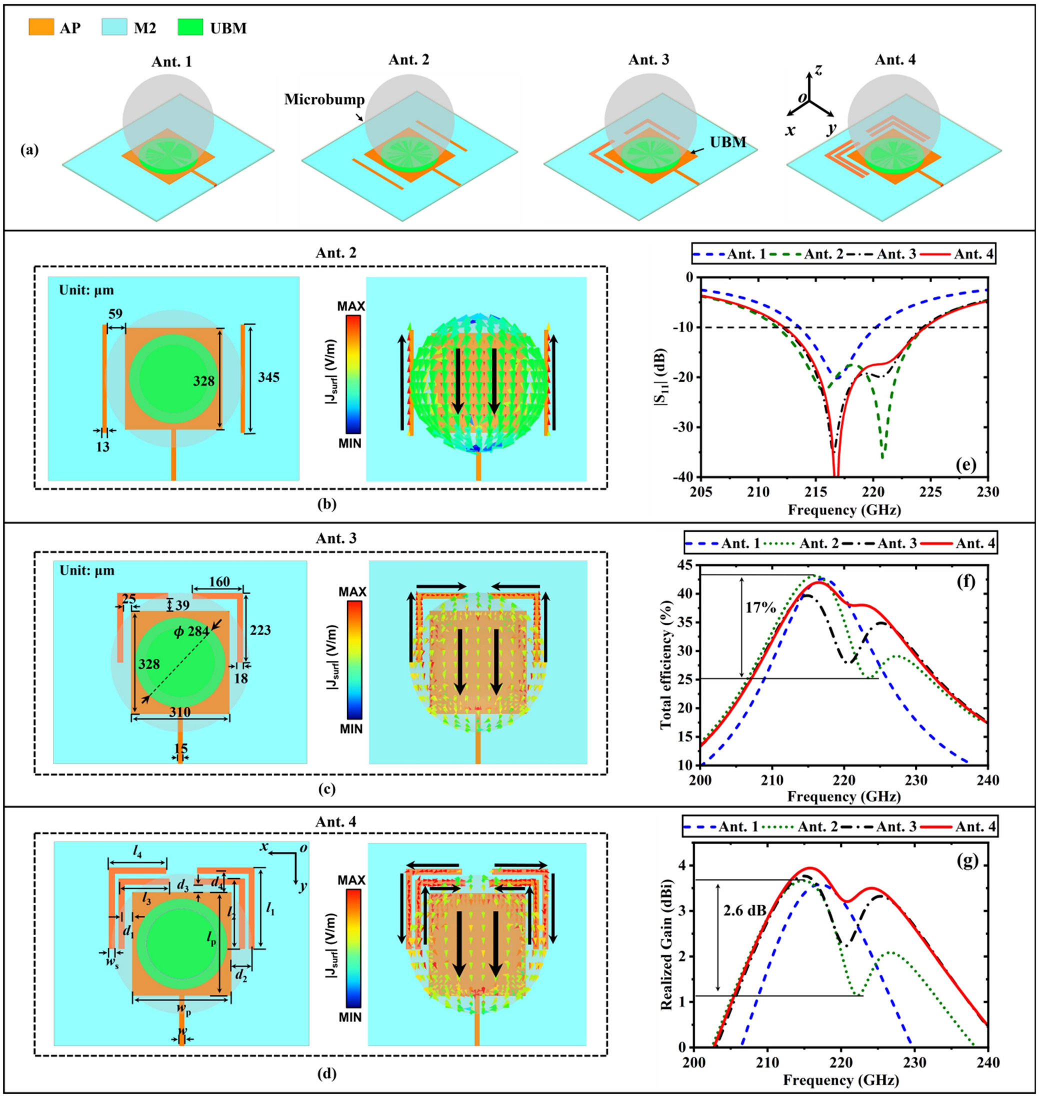


Fig. 3. (a) Evolution of the proposed antenna from Ant. 1 to Ant. 4. (b)–(d) Top views and current distributions of Ant. 2–Ant. 4 at 220 GHz. (e) Simulation results of the reflection coefficients for Ant. 1-4.(f) Simulated total efficiency of Ant. 1–Ant. 4. (g) Simulated realized gain of Ant. 1–Ant. 4.

TABLE I
DETAILED DIMENSIONS (UNIT: MICROMETER)

| Parameter | Value | Parameter | Value | Parameter | Value |
|---|---|---|---|---|---|
| $l_1$ | 257 | $l_2$ | 219 | $w_s$ | 18 |
| $d_1$ | 34 | $d_2$ | 64 | $l_p$ | 329 |
| $d_3$ | 33 | $d_4$ | 68 | $w_p$ | 310 |
| $l_3$ | 164 | $l_4$ | 179 | $w$ | 22 |

Furthermore, two additional strips are placed outside the original parasitic strips, as shown in Fig. 3(d). The detailed dimensions of the antenna structure are summarized in Table I . Fig. 3(d) also shows the simulated current distribution of Ant. 3 at 220 GHz. It can be observed that each pair of parasitic strips operates in differential mode, with the inner and outer strips carrying out-of-phase currents. Notably, at this moment, the currents on the outer parasitic strips are in phase with those on the microbump, resulting in in-phase radiation. Compared to Ant. 3, the efficiency dip at 220 GHz is significantly mitigated, with the total efficiency improving from 28% to 38% , while the antenna gain increases from 2.2 to 3.3 dBi. This improvement confirms the effectiveness of the added outer parasitic strips in suppressing radiation cancellation. However, a slight reduction in efficiency still persists at 220 GHz. This residual loss is primarily attributed to the remaining out-of-phase current distribution between the inner parasitic strips and both the outer strips and the microbump.

Furthermore, it can be observed that although the parasitic strips are highly lossy, the introduced parasitic mode exhibits an efficiency comparable to that of the $HEM_{11}$ mode of the microbump, as shown in Fig. 3(e). This is because the microbump, with lower current loss, remains the dominant radiator in both modes, while the parasitic strips mainly introduce an additional resonant loop. As shown in Fig. 4(a), the gap between the parasitic strips and the patch is modeled as a series capacitor $C_{pn}$ and inductor $L_{pn}$, forming the equivalent circuit in Fig. 4(b). In this model, $R_m$ denotes the radiation resistance of the intrinsic $HEM_{11}$ mode, and losses are neglected for simplicity. As a result, the parasitic and intrinsic resonant circuits share

TABLE II
PERFORMANCE COMPARISON OF EXISTING AOC SOLUTIONS USING STANDARD SEMICONDUCTOR PROCESS

| Ref. | Freq. [GHz] | Antenna type | Efficiency [%] | Bandwidth [%] | Substrate Thickness (ST) | Average Efficiency ×Bandwidth/ST [% /$\lambda_0$] | Gain [dBi] | Antenna Aera [$\lambda_0^2$] | Process |
|---|---|---|---|---|---|---|---|---|---|
| [5] | 300 | Patch + Superstrate | 13* | 2 | 0.009$\lambda_0$ | 28 | 1 | 0.37×0.24 | 65nm CMOS |
| [8] | 270 | SIW Cavity | 21* | 9.3 | 0.009$\lambda_0$ | 200 | -0.5 | 0.36×0.36 | 65nm CMOS |
| [9] | 425 | Patch | 13* | 19 | 0.013$\lambda_0$ | 175 | 1.2 | 0.55×0.55 | 65nm CMOS |
| [15] | 152 | Patch | 12* | 7 | 0.006$\lambda_0$ | 129 | -1.2 | 0.27×0.17 | 130nm BiCMOS |
| [10] | 267 | Annular Ring | 25* | 6.5 | 0.008$\lambda_0$ | 187 | 0.2 | 0.40×0.54 | 130nm SiGe |
| [25] | 323 | Microbump | 32* | 7.5 | 0.009$\lambda_0$ | 258 | 3.8 | 0.34×0.34 | 40nm CMOS |
| [22] | 283 | Microbump | 41.1* | 2.7 | 0.009$\lambda_0$ | 124 | 8.67 | 0.85×0.28 | SG13 BOEL SiGe |
| **This work** | **220** | Microbump w/o Parasitic Elements | 42* | 2.8 | 0.006$\lambda_0$ | 197 | 3.5 | 0.29×0.29 | **65nm CMOS** |
| | | **Microbump with Parasitic Elements** | **42*** | **5.7** | **0.006$\lambda_0$** | **374** | **3.92** | **0.32×0.32** | |

$\lambda_0$: Wavelength at the center frequency. *: Simulated peak radiation efficiency.

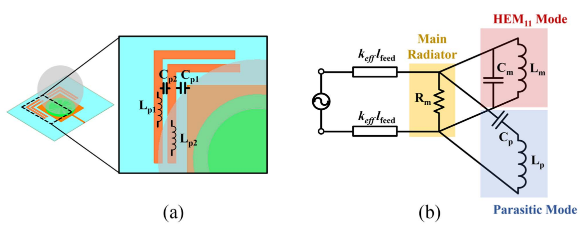


Fig. 4. (a) Equivalent circuit elements introduced by the parasitic strips. (b) Lossless equivalent circuit model of Ant. 4.

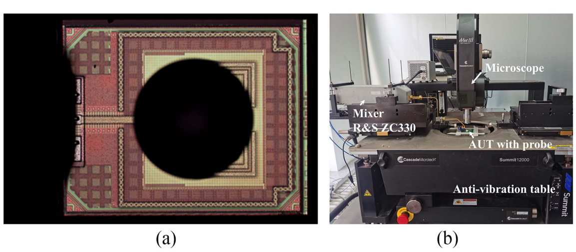


Fig. 5. (a) Microscopic view of the fabricated AoC structure. (a) Photograph of the setup used for measuring the reflection coefficient.

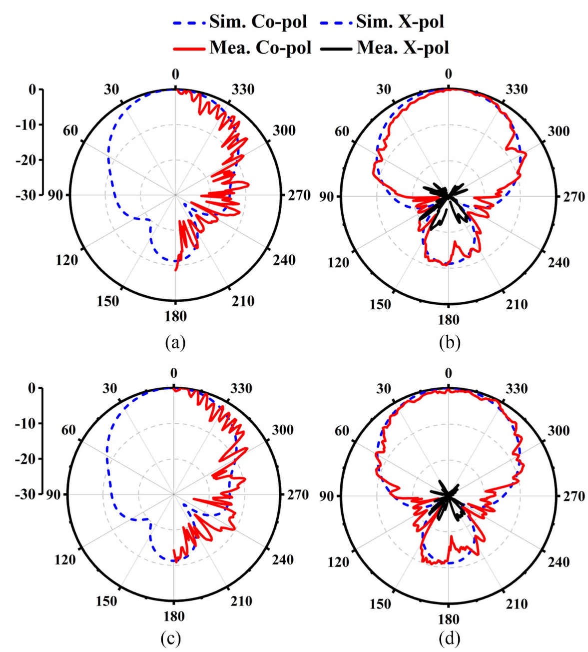


Fig. 6. Simulated and measured normalized radiation patterns: (a) E-plane (*yoz* plane) at 215 GHz, (b) H-plane (*xoz* plane) at 215 GHz, (c) E-plane at 220 GHz, and (d) H-plane at 220 GHz.

the same radiation resistance, enabling comparable radiation efficiency.

## IV. FABRICATION AND VALIDATION

To verify the design, a prototype is implemented using the TSMC 65-nm CMOS technology and flip-chip technology. As shown in Fig. 5(a), the footprint of the AoC is 436 × 436 $\mu m^2$, corresponding to approximately 0.32 $\lambda_0$ × 0.32 $\lambda_0$. The S-parameters of the fabricated AoC were measured using a vector network analyzer with frequency extension modules covering the bands below and above 220 GHz, together with GSG probes. A short-open-load-thru (SOLT) calibration was performed to remove systematic measurement errors. The measurement setup is shown in Fig. 5(b).

Due to mechanical constraints, measurement in the *yoz* plane is limited to –180° to 0°. The measured normalized E-plane and H-plane radiation patterns at 215 GHz are presented in Fig. 6(a) and (b). As observed, the measured patterns exhibit close agreement with the simulated results. The E-plane pattern shows noticeable ripples due to probe-induced reflections and scattering, as the GSG probe behaves as an electrically large structure at these frequencies, leading to multipath effects [26]. The measured radiation patterns of the antenna at 220 GHz in the E-plane and H-plane are shown in Fig. 6(c) and (d), respectively. The radiation characteristics remain consistent with those at 215 GHz. Furthermore, it can be observed that within the 3-dB beamwidth, the cross-polarization level relative to the copolarization is below −23 dB.

The measured $S_{11}$ and gain are shown in Fig. 7. A slight discontinuity in $S_{11}$ appears around 220 GHz due to the use of different probes and frequency extension modules. The measured

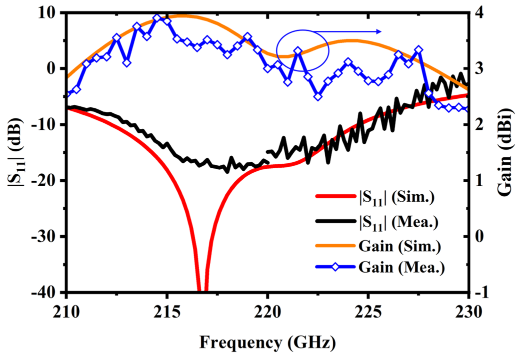


Fig. 7. Simulated and measured results of reflection coefficient and gain curve.

impedance bandwidth is slightly narrower than in simulation, mainly attributed to the lack of a customized thru-reflect-line (TRL) calibration kit for pad de-embedding. In addition, the measured gain curve shows that the antenna achieves a peak gain of 3.85 dBi at 214.5 GHz, corresponding to the $HEM_{11}$ mode of the microbump. At 220 GHz, the antenna gain is 3 dBi, corresponding to the parasitic mode. The bandwidth, radiation efficiency, and gain of on-chip antennas implemented using standard semiconductor processes are summarized in Table II. Under ultra-thin substrate conditions, the proposed microbump antenna achieves a higher efficiency of 42% and a wider measured bandwidth of 5.7% than existing designs. Consequently, it attains the highest value of "Average Efficiency $\times$ Bandwidth/Substrate Thickness (ST)" among reported on-chip antennas. Although the design in [22] achieves higher gain by loading two microbumps on a dipole, it requires a significantly larger chip area. By contrast, the proposed antenna occupies only 0.32 $\lambda_0$ $\times$ 0.32 $\lambda_0$, making it well suited for array implementations.

## V. Conclusion

In this article, a high-efficiency and broadband microbump antenna is proposed, along with a feasible design approach that enables bandwidth and efficiency enhancement for on-chip microbump antennas without requiring any additional postprocessing. By adding two pairs of parasitic strips and configuring them to operate in differential mode, the in-band efficiency is further improved. Crucially, the microbump consistently functions as the dominant radiator at both the $HEM_{11}$ mode resonance and the parasitic mode resonance frequencies. This method effectively addresses the issues of narrow bandwidth commonly encountered in microbump antennas fabricated on ultra-thin substrates.

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